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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEON KUO-LIANG PENG and HENRY D. FALK

Appeal 2009-008763[1]
Application 11/184,316
Technology Center 2400

Before JOSEPH L. DIXON, JEAN R. HOMERE, and THU A. DANG, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

[1] The real party in interest is SIRF Technology, Inc. (App. Br. 2.)

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) (2002) from the Examiner's final rejection of claims 8-25. Claims 1-7 have been canceled. (App. Br. 2.) We have jurisdiction under 35 U.S.C. § 6(b) (2008).

We reverse.

Appellants' Invention

Appellants invented a processor in a global positioning system (GPS) having a first and second modes of operation, wherein the first mode of operation (e.g. acquisition mode) contains a greater number of active correlators than the second mode of operation (e.g. tracking mode). (Spec. 6, ll. 25-29). Upon receiving an input signal (Q) along with a predetermined code (I), each correlator (50) outputs a data stream representing the product of the signal-code pair (IQ- 49) to an accumulator (54), which integrates the out data streams over a predetermined period of time, and forwards the integration sums to a memory circuit (53, 54) for storage. The memory circuit (53, 54) subsequently reallocates memory spaces previously allocated for integration sums corresponding to data streams of correlators that are active in the first mode of operation, and not in the second mode of operation. (Fig. 4, Spec. 5, l. 21-29, Spec. 7, l. 1-11.)

Illustrative Claim

Independent claim 8 further illustrates the invention. It reads as follows:

> 8. A processor in a GPS signal receiver having a first mode of operation and. a second mode of operation, comprising:

> a plurality of correlators, wherein the number of correlators that are active during the first mode of operation is greater than the number of correlators that are active during the second made of operation, and wherein each correlator (1) receives a predetermined code and an input data stream representing digitized signals received from GPS satellites, and (2) provides an output data stream representing a product of the input data stream and the predetermined code, offset by a code phase selected for that correlator;
>
> an accumulator which receives the output data streams of the correlators and which provides, for each data stream, a corresponding integration sum over a predetermined time period; and
>
> a memory circuit which receives and stores the integration sums from the accumulator wherein, during the second mode, memory space allocated for storing the integration sums corresponding to data streams from correlators that are active during the first mode, but not active during the second mode, are reallocated for use other than storing integration sums.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Intrater	5,590,357	Dec. 31, 1996
Turney	5,606,670	Feb. 4, 1997
Baranyai	4,481,624	Nov. 6, 1984
Hyatt	5,168,456	Dec. 1, 1992

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

1. Claims 8, 11, 13-16, 17, 20, 22-25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Turney and Baranyai.

2. Claims 9, 10, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Turney, Baranyai, and Hyatt.

3. Claims 12 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Turney, Baranyai, and Intrater.

Appellants' Contentions

Appellants contend that Baranyai does not teach or suggest a memory circuit that stores integration sums received from accumulators to thereby re-allocate memory spaces allocated for storing integration sums corresponding to correlator data active during the first mode of operation, and inactive during the second mode of operation, as recited in independent claim 1. (App Br. 5-6.) According to Appellants, Baranyai teaches combining the output, a sample RAM with that of an accumulator. (*Id*. at 6.) Appellants argue, however, that the sample RAM only stores input data, but never stores anything from the accumulators. (*Id*.)

Examiner's Findings and Conclusions

The Examiner finds that Baranyai's disclosure of a sample RAM having a plurality of time slot addresses for sharing and reusing memory spaces between two accumulators teaches the memory circuit for re-allocating memory spaces, as recited in independent claim 8. (Ans. 10.) In

particular, the Examiner finds that Baranyai discloses assigning each time one of the slots to either a conference mode, a broadcast mode, or a monitor mode to subsequently store therein results from the accumulators. Therefore, the memory slot is not being used in other modes when it is being used in a particular mode. (*Id*.)

II. ISSUE

Have Appellants shown that the Examiner erred in finding that Baranyai teaches or suggests a memory circuit that stores integration sums received from accumulators to thereby re-allocate memory spaces allocated for storing integration sums corresponding to correlator data active during the first mode of operation, and inactive during the second mode of operation, as recited in independent claim 8?

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

1. Baranyai discloses a system that has a linear time division multiplexed conferencer that continuously sums and outputs a plurality of message samples to 256 sequential time slots integrated into a single chip. (Abst.) The conferencer shares a sample memory between two accumulator's memories to reduce memory requirements by allowing a previously stored message sample to be pre-fetched prior to storing therein a new message sample. (Col. 2, ll. 26-29, ll. 61-65.)

2. The conferencer (100) stores linearly encoded and summed data samples in the accumulators (510, 520) respective to corresponding time slots. In particular, the conferencer (100) includes a RAM control circuit (1600) for holding first and second RAM memory addresses corresponding to first and second time slots. The first address and time slot are used to store the summed message samples in the first or second accumulator (510, 520) whereas the second time slot and corresponding address are used to pre-fetch the summed data samples in the RAM latch (620). Alternatively, the summed message samples are stored in the first time slot and addresses are loaded into the latch. (Col. 3, ll. 35-53, Fig. 1.)

3. The conferencer (100) stores encoded voice samples in time slots corresponding memory addresses in the sample RAM (610). (Col. 4, ll. 45-47.)

IV. ANALYSIS

Independent claim 8 requires, *inter alia*, a memory circuit that stores integration sums received from accumulators to thereby re-allocate memory spaces allocated for storing integration sums corresponding to correlator data is active during the first mode of operation, and inactive during the second mode of operation.

As set forth in the Findings of Fact section, Baranyai discloses a RAM control circuit for allowing a first and second accumulator to store summed data messages in a first and second memory address corresponding to a first and second time slot in such a way when one of the time slots is being used to store a summed message in the accumulator, the other is used to prefetch

the summed message and load it into the RAM latch. (FF. 2) We agree with Appellants that the results of the accumulators are stored in the RAM latch, and not the sample RAM, which only stores encoded input voice samples in its memory addresses and respective time slots. (FF. 3.) While Baranyai's RAM latch teaches a memory circuit that stores in time slots and corresponding memory addresses integration sums received from the accumulators, we do not find any teaching or suggestion in the cited reference of a re-allocation for purposes other than data storage in a second mode inactive memory addresses/time slots that were active in a first mode. Thus, while Baranyai's time slots are being used for storing summed data in memory addresses of the accumulators and the RAM latch, there is no indication that some of these time slots were previously active in a first mode, and have been re-allocated in a second mode when they became inactive. To somehow conclude that the cited re-allocation of the time slots could be accomplished in the RAM latch disclosed in Baranyai would require us to stretch the reference beyond reasonable limits. Further, Turney was not relied upon to cure these deficiencies. Since Appellants have shown at least one error in the Examiner's rejection of claim 8, we need not address Appellants' other arguments. It therefore follows that Appellants have shown that the Examiner erred in concluding that the combination of Turney and Baranyai renders independent claim 8 unpatentable.

Since claims 9-25 recite the limitations of claim 8 discussed above, and neither Hyatt nor Intrater cures the noted deficiencies, we find that

Appellants have shown error in the Examiner's rejection of these claims for the same reasons set forth above.

V. SUMMARY

Appellants have established that the Examiner erred in rejecting claims 8-25 as being unpatentable under 35 U.S.C. § 103(a). We therefore reverse the Examiner's rejections.

REVERSED

Vsh