UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/280,186	11/16/2005	Samantha Regini	NUM.0193US	8060

76446 7590 01/31/2011

Trop, Pruner & Hu, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057-2631

EXAMINER	
CHEN, KIN CHAN	

ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
01/31/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAMANTHA REGINI and
SIMONE ALBA

Appeal 2009-013524
Application 11/280,186
Technology Center 1700

Before PETER F. KRATZ, JEFFREY T. SMITH, and
MICHAEL P. COLAIANNI, *Administrative Patent Judges*.

COLAIANNI, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

This is a decision on an appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 26 through 60, which are all of the claims pending in the above-identified application. We have jurisdiction pursuant to 35 U.S.C. § 6.

We AFFIRM.

STATEMENT OF THE CASE

The subject matter on appeal is directed to a process for defining integrated circuits on a wafer. Claim 26 is illustrative.

> 26. A process for defining integrated circuits on a wafer comprising:
>
> forming at least one silicon semiconductor layer on a substrate having a silicon native oxide layer thereon;
>
> masking the at least one silicon semiconductor layer with a photoresist layer that is photosensitive to photolithography at less than 248 nm;
>
> defining a lithographic pattern in the photoresist layer;
>
> hardening the photoresist layer with a plasma of an inert gas; and
>
> transferring the lithographic pattern onto the wafer using a dry etching with a plasma of a reactive gas, the transferring comprising an initial dry etching using a plasma of a chlorinated gas and the inert gas for removing at least a portion of the silicon native oxide layer while not altering the hardened photoresist layer.

The Examiner maintains the following rejections:

1) Claims 26-60 under 35 U.S.C. § 103(a) as unpatentable over Nagarajan (US 2003/0219683A1, published Nov. 27, 2003) in view of

Doshita (US 2003/0235987 A1, published Dec. 25, 2003) as evidenced by Demmin (US 6,635,185 B2, issued Oct. 21, 2003); and

2) Claim 26-60 under 35 U.S.C. § 103(a) as unpatentable over Vassalli (US 6,495,455 B2, issued Dec. 17, 2002) or Ko (US 2003/0003407 A1, published Jan. 2, 2003) in view of Fong (US 5,812,403, issued Sep. 22, 1998) as evidenced by Demmin and Nagarajan.

REJECTION (1): The rejection over Nagarajan in view of Doshita as evidenced by Demmin.

ISSUE

Did the Examiner err in determining that the applied prior art references would have suggested a process for defining integrated circuits on a wafer comprising, *inter alia*, an initial dry etching step using a plasma of chlorinated gas and inert gas for removing a portion of the silicon native oxide layer while not altering the hardened photoresist layer as required by claims 26 and 50? We decide this issue in the negative.

PRINCIPLES OF LAW

If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

"A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from

the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994).

ANALYSIS AND CONCLUSION

Appellants argue that the combination of applied prior art references would not have suggested a photoresist layer hardened with a plasma of an inert gas as required by claims 26 and 50. (App. Br. 5 and 6). Specifically, Appellants argue that Doshita teaches that "[its] hardened mask of silicon oxide or silicon nitride . . . is not formed then hardened with a plasma of an inert gas thereafter, but is rather formed as a hardened mask." (App. Br. 6).

This argument fails to address and thus fails to show error in the Examiner's stated case, which is based on, *inter alia*, using Nagarajan's hardenable photoresist formed on a polysilicon layer, and employing the well known step of removing a silicon native oxide layer on a polysilicon film via a plasma of chlorinated gas and inert gas as evidenced by Doshita. (*See* Ans. 3-6; *see also* Nagarajan, ¶ [0019] and Doshita, ¶ [0180]).

Appellants further argue that "Doshita teaches away from its selective combination with Nagarajan et al. because the application of Doshita's dry etching . . . to Nagarajan, without the feature of not altering the hardened photoresist layer, would render the combination inoperable." (App. Br. 6). In that regard, Appellants argue that "since sputtering results in a shape change of the photoresist and Doshita discloses a method whereby etching is accomplished primarily by sputtering, the application of Doshita to Nagarajan . . . would alter the photoresist and produce . . . [a] trapezoidal wear pattern, and a resulting inoperable memory cell." (App. Br. 7). In doing so, Appellants argue that "the application of . . . [Doshita's] dry

etching process to a silicon native oxide layer masked with a hardened photoresist . . . would render an unusable device." (App. Br. 7).

With respect to Appellants' inoperability argument, Appellants have not provided us with any credible evidence[2] or persuasive argument to show that employing the well known step of removing a silicon native oxide layer on a polysilicon film via a plasma of chlorinated gas and inert gas as evidenced by Doshita in Nagarajan's semiconductor fabrication method would have "render[ed] an unusable device."

In addition, with respect to Appellants' teaching away argument, while Doshita, in a preferred embodiment, teaches the use of a hard mask, nowhere does Doshita discourage employing its step of removing a silicon native oxide layer in a semiconductor fabrication process method that uses a hardenable photoresist. *Gurley*, 27 F.3d at 553. Thus, Appellants' argument is unpersuasive of reversible error.

Appellants argue for the first time in the Reply Brief that Nagarajan "does not harden the photoresist before etching, but claims that he hardens the resist during etching. As a result it is unavoidable that Nagarajan damages his photoresist . . . [and thus] is incapable of meeting the limitation of claim 26 'while not altering the hardened photoresist layer.'" (Reply Br. 1). We need not consider this new argument since it was not raised in the opening Brief.[3]

---

[2] Appellants cite to the Vahedi article on page 7 of the Appeal Brief. Appellants have not established that Vahedi's dry etchant or conditions are the same as Doshita's or Nagarajan's. Therefore, it is not possible to determine whether Vahedi's change in shape argued by Appellants would have occured in Doshita's and Nagarajan's etching process.

[3] *See Ex parte Nakashima*, 93 USPQ2d 1834, 1836-40 (BPAI 2010) (Nonprecedential).

In any event, it is manifest that the relevant etching step that occurs after hardening the resist is an etching step associated with the lithographic pattern transfer onto a wafer as indicated in both independent claims on appeal. The belated argument in the Reply Brief does not address the timing of the relevant pattern transfer etching step taught or suggested by Nagarajan. Nagarajan discloses that pattern transfer etching occurs subsequent to hardening and trimming the resist layer. See Nagarajan at paragraphs 0019 and 0047.

Thus, it follows that the Examiner did not err in determining that the applied prior art references would have suggested a process for defining integrated circuits on a wafer comprising, *inter alia*, an initial dry etching step using a plasma of chlorinated gas and inert gas subsequent to hardening the resist while not altering the hardened photoresist layer as required by claims 26 and 50.

Accordingly, we affirm the Examiner's decision to reject claims 26-60 under 35 U.S.C. § 103(a) over Nagarajan in view of Doshita as evidenced by Demmin.

REJECTION (2): The rejection over Vassalli in view of Fong as evidenced by Demmin and Nagarajan.

Appellants argue that

> Vassalli et al. expressly teaches away from its combination of Fong et al. . . . [as] Vassalli et al. states that "[i]t has been ascertained, moreover, that where even a small amount of

> chemically reactive gas to the layer to be etched is introduced, the effectiveness of the technique has been lost."

(App. Br. 8-9). In this regard, Vassalli teaches that this layer to be etched may be a polycrystalline silicon, which is positioned above a wafer. (Vassalli, col. 1, ll. 26-31 and 49-52; and col. 2, ll. 24-30).

The Examiner, however, fails to respond to Appellants' teaching away argument. In this regard, the Examiner does not explain why it would have been obvious to employ Fong's plasma of inert gas and chlorine-containing gas, which are known to be chemically reactive, to remove a silicon native oxide layer on Vassalli's wafer in view of Vassalli's teaching that "the effectiveness of the technique has been lost" when "even a small amount of chemically reactive gas" is introduced to its polycrystalline silicon, which is positioned above its wafer.

Thus, it follows that the Examiner erred in determining that the applied prior art references would have suggested the inventions required by claims 26 and 50. We reverse the Examiner's decision to reject claims 26-60 under 35 U.S.C. § 103(a) over Vassalli in view of Fong as evidenced by Demmin and Nagarajan.

REJECTION (2): The rejection over Ko in view of Fong as evidenced by Demmin and Nagarajan.

Appellants argue that

> the selective combination of Ko et al. and Fong et al. fails to disclose an initial dry etching using a plasma of a chlorinated gas and the insert gas for removing at least a portion of the silicon native oxide layer <u>while not altering the hardened photoresist layer</u>. As stated in Ko et al., "[t]he thickness of the hardened [photoresist] layer has been decreased through the

> etching process." (paragraph 35). Moreover, Ko et al. discloses that "[t]he etch rate of the hardened layer is smaller than the etch rate of the non silicon-containing photoresist." (paragraph 37). Thus, the combination of Ko et al. and Fong et al. fails to disclose the above noted feature.

(App. Br. 9).

This argument, however, fails to address and thus fails to show error in the Examiner's stated case, which is based on, *inter alia*, the inherency of this claimed characteristic. (*See* Ans. 9-10).

In this regard, while Ko at paragraphs 35 and 37 teaches that the thickness of its hardened layer is decreased via etching, Appellants do not direct us to any credible evidence or provide any persuasive explanation to show how Ko's etching step uses a plasma of chlorinated gas and inert gas as required by claims 26 and 50. In other words, Appellants fail to show that the thickness of Ko's hardened layer will decrease when the relevant etching of Ko is accomplished using a plasma of chlorinated gas and inert gas as taught by Fong. Accordingly, Appellants' arguments are without persuasive merit.

Thus, it follows that the Examiner did not err in determining that the applied prior art references would have suggested the inventions required by claims 26 and 50.

Accordingly, we affirm the Examiner's decision to reject claims 26-60 under 35 U.S.C. § 103(a) over Ko in view of Fong as evidenced by Demmin and Nagarajan.

ORDER

In summary, we sustain the Examiner's rejection (1) over Nagarajan in view of Doshita as evidenced by Demmin and rejection (2) over Ko in view of Fong as evidenced by Demmin and Nagarajan.

We reverse the Examiner's rejection (2) over Vassalli in view of Fong as evidenced by Demmin and Nagarajan.

Accordingly, the Examiner's decision is affirmed.

TIME PERIOD

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED

bar

TROP, PRUNER & HU, P.C.
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631