UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDRE MARIA FRANCOIS COLLIGNON
and KOENRAAD PIETER LODEWIJK VAN NIEUWENHOVE

Appeal 2009-007831
Application 11/220,911
Technology Center 2100

Decided: January 28, 2010

Before JAY P. LUCAS, ST. JOHN COURTENAY III, and
DEBRA K. STEPHENS, *Administrative Patent Judges.*

COURTENAY, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-20. We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing on this appeal was conducted on Thursday, January 21, 2010. We Reverse.

STATEMENT OF THE CASE

THE INVENTION

Appellants' invention relates generally to the field of data processing systems. More particularly, the invention on appeal is directed to "data processing systems having a plurality of data path elements operable independently to perform in parallel respective data processing operations specified by a program instruction, such as, for example, a so called very long instruction word (VLIW) and measures to reduce program code size for such systems. (Spec. 2).

Independent claim 1 is illustrative:

> 1. A method of generating at least one instruction set from a plurality of program instructions, said plurality of program instructions comprising a plurality of instruction fields each of said instruction fields operable on decoding to generate control signals for transmission by individual command buses, said method comprising the steps of:
>
> determining which combination of command buses each instruction is operable to communicate control signals to and forming a cluster of instructions from instructions that communicate control signals to a same combination of command buses;
>
> developing at least one instruction set for at least some of said instruction clusters, said at least one instruction set having fewer bits than said program instruction;
>
> specifying a number of identification bits within said at least one instruction set operable to identify said instruction set;

> determining a number of bits required for each instruction field within said at least one instruction set to specify all possible control signals that can be sent by said at least one instruction set along a respective one of said command buses and reallocating any bits that are allocated to said instruction field that are in excess of said determined required number to said identification bits, such that an increased number of different instruction sets can be identified by said identification bits.

THE REFERENCES

The Examiner relies upon the following references as evidence:

Tsushima	US 6,044,450	Mar. 28, 2000
Ohtsu	US 5,574,913	Nov. 12, 1996
Tanner	US 4,295,218	Oct. 13, 1981

THE REJECTIONS

1. The Examiner rejected claims 1-6, 9-16, 19, and 20 under 35 U.S.C. §102(b) as anticipated by Tsushima.
2. The Examiner rejected claims 7 and 17 under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsushima and Ohtsu.
3. The Examiner rejected claims 8 and 18 under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsushima, Ohtsu, and Tanner.

Contentions by Appellants

Appellants contend, *inter alia*, that Tsushima does not disclose

> "reallocating any bits that are allocated to said instruction field that are in excess of said determined required number to said

> identification bits, such that an increased number of different instruction sets can be identified by said identification bits."

(App. Br. 12-13; *see* independent claim 1 and commensurate language recited in independent claim 12).

The Examiner's Response

> The Examiner disagrees:
>
> In response the examiner respectfully asserts that the bits of the instruction fields (see e.g. fig. 2 ele. 1-7a) are reallocated to create a compressed instruction (see e.g. fig. 2c). That is, the excess bits of the longer series of smaller instructions are reallocated to create compressed identification bits. Appellant[s] ha[ve] agreed that the compression results in a shorter instruction. In order for the identification bits to be shorter than the original instructions, there clearly is a reallocation of "excess bits".

(Ans. 12-13).

Reply Brief Response

> As pointed out in the Appeal Brief on page 13, Appellants notes and agrees that Tsushima teaches that group codes are used when several small instructions are compressed to form a group. However, as pointed out in the Brief, Tsushima does not disclose any reallocation, i.e., the changing of excess bits into identification bits. Tsushima merely discloses the production of a shorter VLIW compressed instruction (*see* column 8, lines 10-15).
>
> The Examiner seems to believe that Appellants' agreement that "compression results in a shorter instruction" somehow automatically teaches reallocation. This is not the case – compression is the shortening of the number of bits rather than the reallocation of bits. Appellants' claims

> specifically requires reallocation of "instruction field bits" (in excess of the required number of identification bits) to "identification bits" so that "an increased number of different instruction sets can be identified by said identification bits." The Examiner, in the Answer, in effect ignores the claim language (regarding the change from instruction field bits to identification bits) and merely argues the well-known fact that a compressed instruction, by definition, results in a shorter instruction. However, there is no indication that in Tsushima's shorter instruction that there is any reallocation of bits in any fashion.

(Reply Br. 5-6).

ISSUE

Based upon our review of the administrative record, we have determined that the following issue is dispositive in this appeal:

> Have Appellants shown the Examiner erred in finding that
>
> Kozakura discloses
>
> "reallocating any bits that are allocated to said instruction field that are in excess of said determined required number to said identification bits, such that an increased number of different instruction sets can be identified by said identification bits."

(*See* independent claim 1 and the commensurate language recited in independent claim 12).

PRINCIPLES OF LAW

"Whether an invention is anticipated is a question of fact." *Elan Pharmaceuticals, Inc. v. Mayo Foundation for Medical Educ. and Research*, 346 F.3d 1051, 1054 (Fed. Cir. 2003) (citing *Hoover Group, Inc.*

v. Custom Metalcraft, Inc., 66 F.3d 299, 302 (Fed. Cir. 1995)). In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the Examiner's proffered prima facie case.

FINDINGS OF FACTS

The Tsushima reference

1. Tsushima discloses:

> FIG. 2C shows the format of a VLIW instruction 100b obtained by compressing in space one time-compressed VLIW instruction having the format shown in FIG. 2B. A grouped instruction is set to each of instruction fields 21, 34, 56 and 7a of this VLIW instruction 100b. For this space compression, a plurality of small instructions in one time-compressed VLIW instruction is divided into a plurality of groups each constituted of a plurality of small instructions, and a plurality of small instructions contained in each group are *compressed* to generate a grouped instruction representative of a group of small instructions. Specifically, in place of OP codes of each group, a group code is set which unanimously determines a combination of the OP codes. This group code has a length shorter than the total length of the OP codes. *Therefore, this group code is a compressed code of the OP codes of small instructions.* The operand information of these small instructions is set in the grouped instruction.

(Col. 7, l. 54 through col. 8, l. 4, emphasis added).

2. Tsushima discloses:

> In this manner, a grouped instruction for a group of small instructions is generated, the grouped instruction including one compressed group code and a plurality of information sets of the small instructions. In addition, the length of the NOP number sub-field of each of a plurality of small instructions of the grouped instruction is shortened properly. Therefore, the length of a VLIW instruction having a plurality of these grouped instructions becomes shorter than the VLIW instruction *compressed* only in time and not in space. This newly generated VLIW instruction is also called a space-*compressed* VLIW instruction where applicable.

(Col. 8, ll. 5-15, emphasis added).

3. Tsushima discloses:

> In this embodiment, for example, the two small instructions in the load/store instruction fields 1a and 2a shown in FIG. 2B are compressed to generate a new grouped instruction (FIG. 2C). For example, the field 21 of the grouped instruction shown in FIG. 2C includes: a sub-field 10A for setting a group code obtained by compressing the OP codes of the small instructions la and 2a; an operand sub-field 11A for setting the operands 11a and 11b of the small instruction 1a; a sub-field 12A for setting the NOP number of the small instruction 1a; an operand sub-field 11B for setting the operands 11a and 11b of the small instruction 2a; and a sub-field 12B for setting the NOP number of the small instruction 2a.

(Col. 8, ll. 15-27).

ANALYSIS

Independent claims 1 and 12

We decide the question of whether Appellants have shown the Examiner erred in finding that Tsushima discloses

> "reallocating any bits that are allocated to said instruction field that are in excess of said determined required number to said

> identification bits, such that an increased number of different instruction sets can be identified by said identification bits."

(*See* independent claim 1 and the commensurate language recited in claim 12).

After considering the evidence before us, and the respective arguments on both sides, we find the Tsushima reference falls short of anticipating Appellants' claimed invention for essentially the same reasons argued by Appellants in the Briefs regarding at least the third argued "reallocation" limitation. In particular, we find the Examiner is incorrectly and unreasonably construing the claimed "reallocation" *of excess bits that are allocated to the instruction field . . . to said identification bits* for the reasons discussed *infra*. (*See* Ans. 13).

We begin our analysis by broadly but reasonably construing the disputed claim term "reallocating" (claim 1) (*cf.* "reallocate" – claim 12). During prosecution, "the PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*. at 1313.

When we refer to Appellants' disclosure for *context*, we find Appellants' use of the claim term "reallocate" is fully consistent with the ordinary and customary meaning of that term at the time of the invention

(i.e., to repurpose). In particular, Appellants' Specification describes the claimed "reallocation" as follows: "An analysis of the width of the instruction field in each instruction set is then made and any bits that it is determined are not required within this field are reallocated as identification bits to identify the instruction set." (Spec. 12, ll. 2-4, underlining added).

Thus, Appellants' invention as disclosed and claimed *reallocates* or repurposes excess bits not required for the instruction field as identification bits operable to identify the instruction set. (*Id.*; *See* Claims 1 and 12).

In contrast, the Examiner relies on Tsushima's disclosure of *compression* to anticipate the claimed *reallocation* of bits, particularly Fig. 2C and the corresponding description found in column 8 of Tsushima. (Ans. 5, ¶1; *see also* Ans. 12-13). We find particular fault with the Examiner's findings in the Answer (describing Tsushima's Fig. 2) that "the excess bits of the longer series of smaller instructions are *reallocated* to create compressed identification bits" and "[i]n order for the identification bits to be shorter than the original instructions, there clearly is a *reallocation* of "excess bits." (Ans. 12-13, emphasis added).

While Tsushima clearly teaches the compression of instructions (FF 1-3), we find nothing in the portion of Tsushima relied on by the Examiner that informs the artisan regarding what becomes of any excess bits that become available as a result of the compression. We find that to affirm the Examiner on this record would require speculation on our part. We decline to engage in speculation.

Simply put, we find that compression is not the same as reallocation.[1]

Therefore, we find the weight of the evidence before us supports Appellants' position as argued in the Briefs regarding at least the third argued "reallocation" limitation of independent claim 1 (and the commensurate language recited in independent claim 12). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986).

Accordingly we reverse the Examiner's anticipation rejection of independent claims 1 and 12, and associated dependent claims 2-6, 9-11, 13-16, 19, and 20 that also stand rejected under § 102. Because we have reversed the Examiner's rejection of each independent claim on appeal, we also reverse the Examiner's § 103 rejections for dependent claims 7, 8, 17, and 18.

CONCLUSIONS

1. Appellants have established the Examiner erred in rejecting claims 1-6, 9-16, 19, and 20 under 35 U.S.C. §102(b) as anticipated by Tsushima.
2. Appellants have established the Examiner erred in rejecting claims 7 and 17 under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsushima and Ohtsu.

[1] We need not reach the issue of whether compression of a long instruction might suggest reallocation of the resulting excess bits, because the Examiner has rejected each independent claim under § 102.

3. Appellants have established the Examiner erred in rejecting 8 and 18 under 35 U.S.C. § 103(a) as unpatentable over the combination of Tsushima, Ohtsu, and Tanner.

ORDER

We reverse the Examiner's decision rejecting claims 1-20.

REVERSED

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