UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL KERSHAW, DONALD FELTON,
ASHLEY MILES STEVENS, and ANTHONY PAUL THOMPSON

Appeal 2009-009308
Application 11/230,498
Technology Center 2100

Decided: February 5, 2010

Before ST. JOHN COURTENAY III, CAROLYN D. THOMAS, and JAMES R. HUGHES, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 2, 7-10, 13-17, 22-25, and 28-30. The Examiner indicates that claims 3-6, 11, 12, 18-21, 26, and 27 would be allowable if

rewritten in independent form. (Ans. 2). We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing on this appeal was conducted on Tuesday, February 2, 2010. We Reverse.

STATEMENT OF THE CASE

INVENTION

Appellants' invention relates to a data processing apparatus and method for controlling access to memory. (Spec. 1). More particularly, the invention on appeal is directed to a "memory management unit [that] produces not only a memory address, but also one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address." (Spec. 3, ll. 18-20).

ILLUSTRATIVE CLAIM

1. A data processing apparatus, comprising:

> main processing logic operable to execute a sequence of instructions in order to perform a process;
>
> subsidiary processing logic operable to perform at least part of said process on behalf of the main processing logic;
>
> a memory accessible by the main processing logic when performing said process, the main processing logic defining a portion of said memory to be allocated memory accessible to the subsidiary processing logic when performing said at least part of said process;
>
> a memory management unit, programmable by the main processing logic, for controlling access to the allocated memory by the subsidiary processing logic, the main processing logic being operable to program the memory management unit such

> that for an access request issued by the subsidiary processing logic relating to the allocated memory, the memory management unit produces a memory address and one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address.

PRIOR ART

Ledebohm	US 7,065,630 B1	Jun. 20, 2006
Applicant's Admitted Prior Art (AAPA)	(Spec. 2, ll. 15-24, "Description of the Prior Art").	

THE REJECTIONS

1. The Examiner rejected claims 1, 2, 7-9, 13-17, 22-24, and 28-30 under 35 U.S.C. § 102(e) as anticipated by Ledebohm.
2. The Examiner rejected claims 10 and 25 under 35 U.S.C. § 103(a) as unpatentable over the combination of Ledebohm and AAPA.

CONTENTIONS BY APPELLANTS

Appellants contend, *inter alia*, that Ledebohm does not disclose the claimed "memory management unit [that] produces a memory address and one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address." (App. Br. 9-11; *see* independent claim 1 and the commensurate language recited in independent claim 16).

THE EXAMINER'S RESPONSE

The Examiner disagrees:

> As shown by Ledebohm in col. 6, lines 48-59, the command issued by CPU 102 includes physical address that can be recognized by the GPU 114 so that the GPU 114 can be delegated to access the Graphics Memory 1 16. Hence, the CPU 102 and its associated logical/programs must be definitively aware that the Graphics Memory 116 is allocated memory accessible to the GPU 114.

(Ans. 13).

REPLY BRIEF RESPONSE

As pointed out in Appellants' previous responses . . .

> [t]he problem discussed in Ledebohm is how to allow the CPU (main processing unit) to occasionally access the graphics memory. As pointed out by the Examiner, and as discussed in our previous responses, this CPU 102 is able to access the graphics memory via an indirect path or a direct path. In both cases, the access requests are initiated from the CPU. When using an indirect path, the CPU issues access requests specifying physical memory addresses, and these are placed in command buffer 124, whereafter the GPU executes the required commands in respect of the graphics memory 116 (*see* column 6, lines 50 to 55).

(Reply Br. 6).

ISSUE

Based upon our review of the administrative record, we have determined that the following issue is dispositive in this appeal:

> Under § 102, have Appellants shown the Examiner erred in rejecting representative claim 1 by finding that Ledebohm discloses or describes the claimed "memory management unit

> [that] produces a memory address and one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address?"

(*See* independent claim 1 and the commensurate language recited in independent claim 16).

PRINCIPLES OF LAW

"Whether an invention is anticipated is a question of fact." *Elan Pharmaceuticals, Inc. v. Mayo Foundation for Medical Educ. and Research*, 346 F.3d 1051, 1054 (Fed. Cir. 2003) (citing *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 299, 302 (Fed. Cir. 1995)). In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the Examiner's proffered prima facie case.

FINDINGS OF FACTS

1. Ledebohm discloses that "[a] memory interface 123 is provided to control access to graphic memory 116." (Col. 4, ll. 8-9).
2. Ledebohm discloses "at various times during its operation, driver program 136 invokes an appropriate function of a resource manager 138 to allocate portions of graphics memory 116 for its own use; after

> allocation, driver program 136 can issue commands to GPU 114 that reference allocated memory locations." (Col. 6, l. 66 through col. 7, l. 4).

3. Ledebohm discloses:

> Graphics memory 116 can be accessed by programs executing on CPU 102 via an indirect path or a direct path. In the indirect path, driver program 136 is used to queue a memory access command in command buffer 124. GPU 114 executes the command and returns an appropriate response. Since these commands are executed by GPU 114, memory locations in graphics memory 116 may be identified using a physical address (e.g., an offset) recognizable by GPU 114. In a direct access path, a command executed by CPU 102 includes a virtual memory address that is mapped to a location in graphics memory 116, enabling CPU 102 to access the location directly.

(Col. 6, ll. 48-59).

ANALYSIS

Independent claims 1 and 16

We decide the question of whether Appellants have shown the Examiner erred in finding that Ledebohm discloses or describes the claimed "memory management unit [that] produces a memory address and one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address." (*See* independent claim 1 and the commensurate language recited in independent claim 16).

After considering the evidence before us, and the respective arguments on both sides, we find the Ledebohm reference falls short of anticipating Appellants' claimed invention. At the outset, we are in agreement with Appellants that the Examiner has not clearly mapped the claimed memory management unit (MMU) with a corresponding structure in

the Ledebohm reference. It is our view that the Examiner paints with an broad brush by reading the claimed memory management unit on nebulous "logic/circuitry that manages indirect and direct access to the Graphics Memory 116" without clearly specifying in the record which particular component in Ledebohm corresponds to Appellants' claimed memory management unit. (Ans. 9, ¶2).

We agree with Appellants that the term "memory management unit" (MMU) is a recognized term of art that corresponds to a hardware device that performs memory management functions. *See* Reply Br. 2-3. We find this broad but reasonable interpretation is fully consistent with Appellants' Specification that describes "peripheral memory management unit (MMU) 50 being interposed between the bus 60 and subsidiary processing units 30, 40." (Spec. 10, ll. 30-31). To the extent that the Examiner relies on Ledebohm's CPU 102 and/or GPU 114 as purportedly providing structure corresponding to the claimed MMU, we find the Examiner has not shown the claimed arrangement, as the Examiner has also read the claimed "main processing logic" on Ledebohm's CPU 102, (Ans. 4), and the claimed "subsidiary processing logic" on Ledebohm's GPU 114 (Ans. 4, 10).[1]

Since the Examiner does not identify the specific hardware component in Ledebohm that corresponds to the claimed MMU, the Examiner appears to be relying on certain memory management functions

[1] To anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001); *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991).

performed by various software components in Ledebohm (*e.g.*, Driver Program 136, and/or Resource Manager 138). (*See* FF 2). We agree that Ledebohm is directed to performing memory management functions.[2] However, we note that functional equivalence is not enough to show anticipation of a structural component (such as the claimed memory management unit). *See In re Ruskin*, 347 F.2d 843, 846 (CCPA 1965) ("the functional equivalent is not enough to be a full anticipation of the specific device claimed by appellant.").

Nevertheless, in reviewing the entirety of the Ledebohm reference, we find Ledebohm discloses that "[a] memory interface 123 is provided to control access to graphic memory 116." (FF 1). We note that memory interface 123 is not depicted in any of Ledebohm's drawings and is not further discussed elsewhere in the reference. Memory interface 123 does not appear to have been considered by the Examiner as a structure that performs MMU functions.

However, even assuming *arguendo* that Ledebohm's memory interface 123 is a structure that performs memory management functions, we find the Examiner has not clearly established in the record how any specific element in Ledebohm corresponds to Appellants' claimed memory management unit that produces: (1) a memory address, and (2) *one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address*," within the meaning of Appellants' independent claims 1 and 16.

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[2] : *See* Ledebohm, col. 1, ll. 7-10: "The present invention relates in general to virtual memory systems and in particular to systems and methods for on-demand *memory management*." (emphasis added).

The Examiner appears to read these two claimed elements on Ledebohm's "command issued by CPU 102 [that] includes [a] physical address that can be recognized by the GPU 114 so that the GPU 114 can be delegated to access the Graphics Memory 116." (Ans. 13). While we agree that Ledebohm discloses a memory address (either physical or virtual), we do not find that the memory access command executed by GPU 114 (FF 3) fairly discloses (2) *one or more associated memory attributes identifying one or more properties of the allocated memory at that memory address,* as required by the express language of Appellants' independent claims 1 and 16.

If the Examiner is broadly reading the claimed *memory attributes* on Ledebohm's direct or indirect methods of accessing memory, we do not find that "direct" or "indirect" accessing of graphics memory 116 (by CPU 102) reasonably *identifies one or more properties of the allocated memory* at a particular memory address because Ledebohm discloses that the same graphics memory 116 can be accessed by programs executing on CPU 102 via an indirect path or a direct path. (FF 3). We note that "absence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.,* 793 F.2d 1565, 1571 (Fed. Cir. 1986).

Accordingly, we reverse the Examiner's anticipation rejection of independent claims 1 and 16, and associated dependent claims 2, 7-9, 13-15, 17, 22-24, and 28-30 that also stand rejected under § 102. Because we have reversed the Examiner's rejection of each independent claim on appeal, we also reverse the Examiner's § 103 rejection for dependent claims 10 and 25.

CONCLUSIONS

1. Appellants have established the Examiner erred in rejecting claims 1, 2, 7-9, 13-17, 22-24, and 28-30 under 35 U.S.C. § 102(e) as anticipated by Ledebohm.
2. Appellants have established the Examiner erred in rejecting claims 10 and 25 under 35 U.S.C. § 103(a) as unpatentable over the combination of Ledebohm and AAPA.

ORDER

We reverse the Examiner's decision rejecting claims 1, 2, 7-10, 13-17, 22-25, and 28-30.

REVERSED

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